The Art of Breaking Things Down - Hierarchical Abstraction for Power Sensitive SoC Signoff

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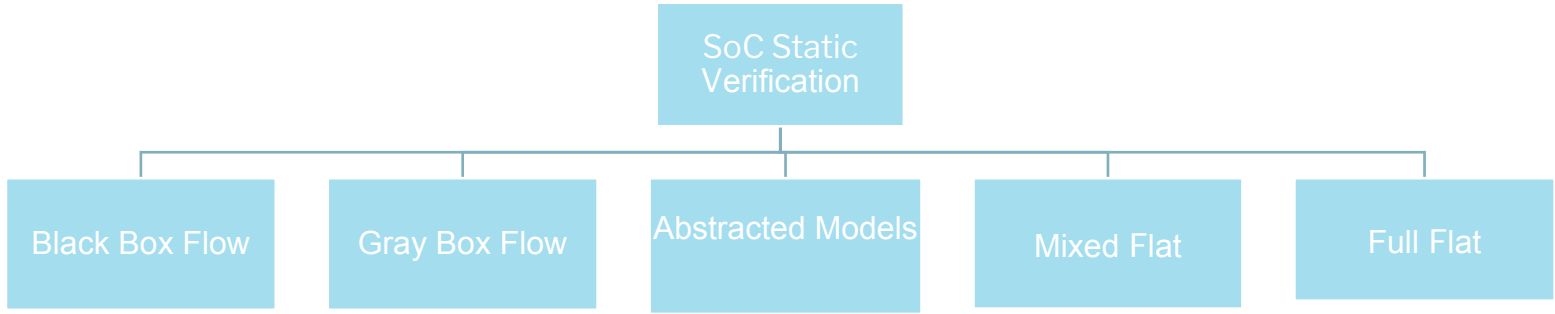
Agenda

- Need for hierarchical verification
- Static Abstraction Model (SAM) and On-The-Fly SAM (OTF SAM)
- Results
- Summary

Need for hierarchical verification

- SoC sign-off runs take 3-4 days for closure due to increased design size/complexity
- BlackBox based hierarchical flow provides good gains in terms of runtime and memory but sign off accuracy is lost
- Abstract model based hierarchical flows provides the ideal trade-off between signoff accuracy and capacity constraints



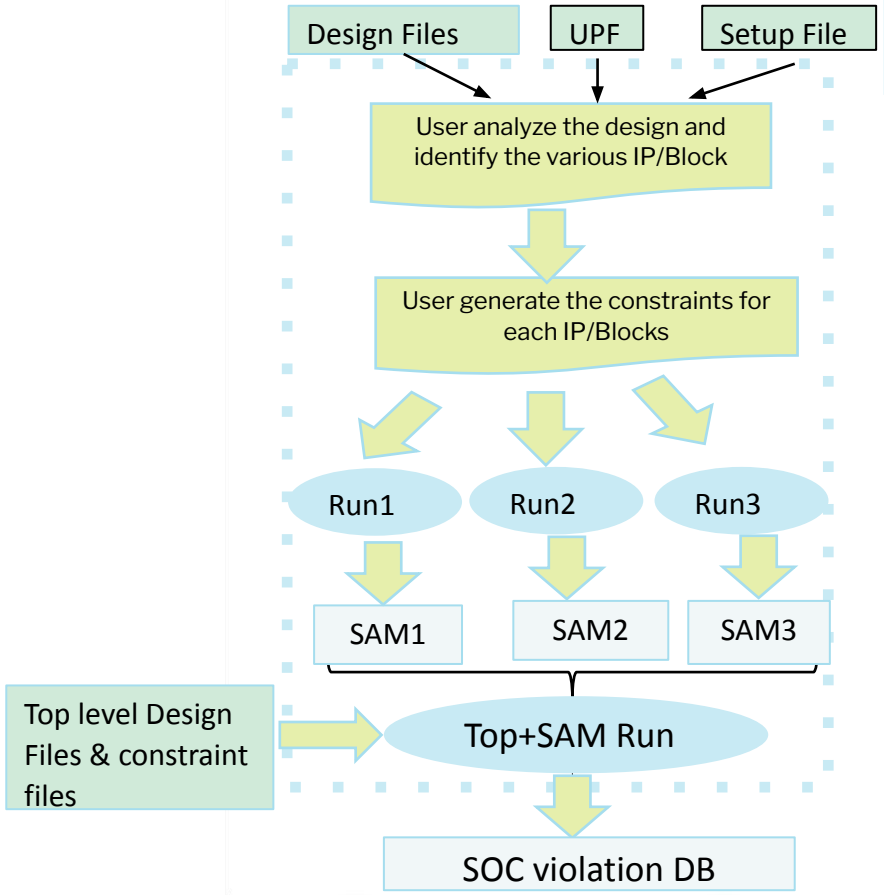
- VC LP hierarchical Abstraction Model is called SAM (Static Abstraction Model)
- Abstract model based hierarchical flows for verification of SOC designs are challenging due to below constraints:
  - Manual identification of block boundaries
  - Complications in creating setup for each identified block from the SoC level setup
  - High TAT of full flow due to sequential processing of each individual block
  - QoR accuracy

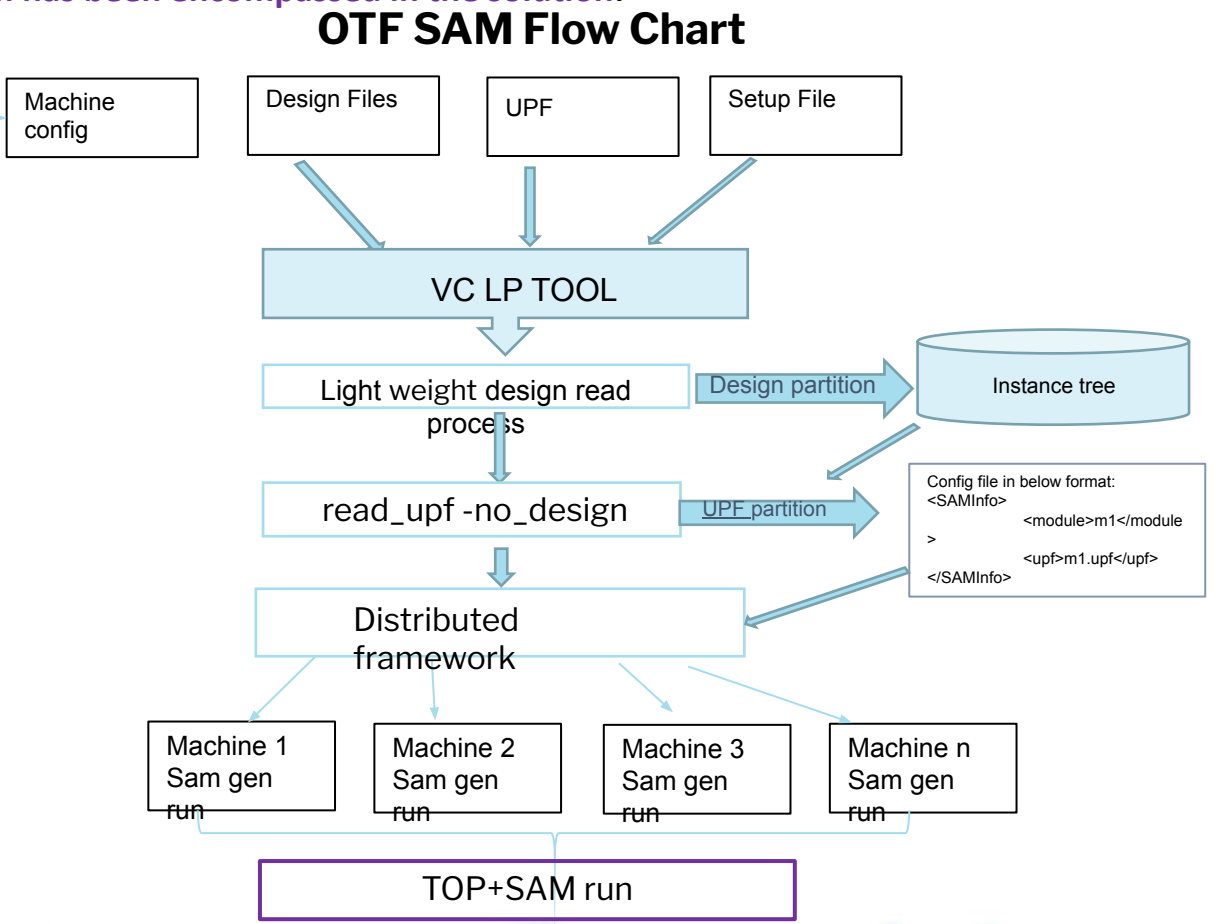
SAM and On-The-Fly SAM

To make the SAM based solution workable at every design house we have developed OnTheFlySAM (OTF) flow with below features:

- Automatic SAM candidate and UPF identification
- Automatic run script generation for each SAM candidate
- Distributed SAM model generation followed by SAM model based SoC sign-off run

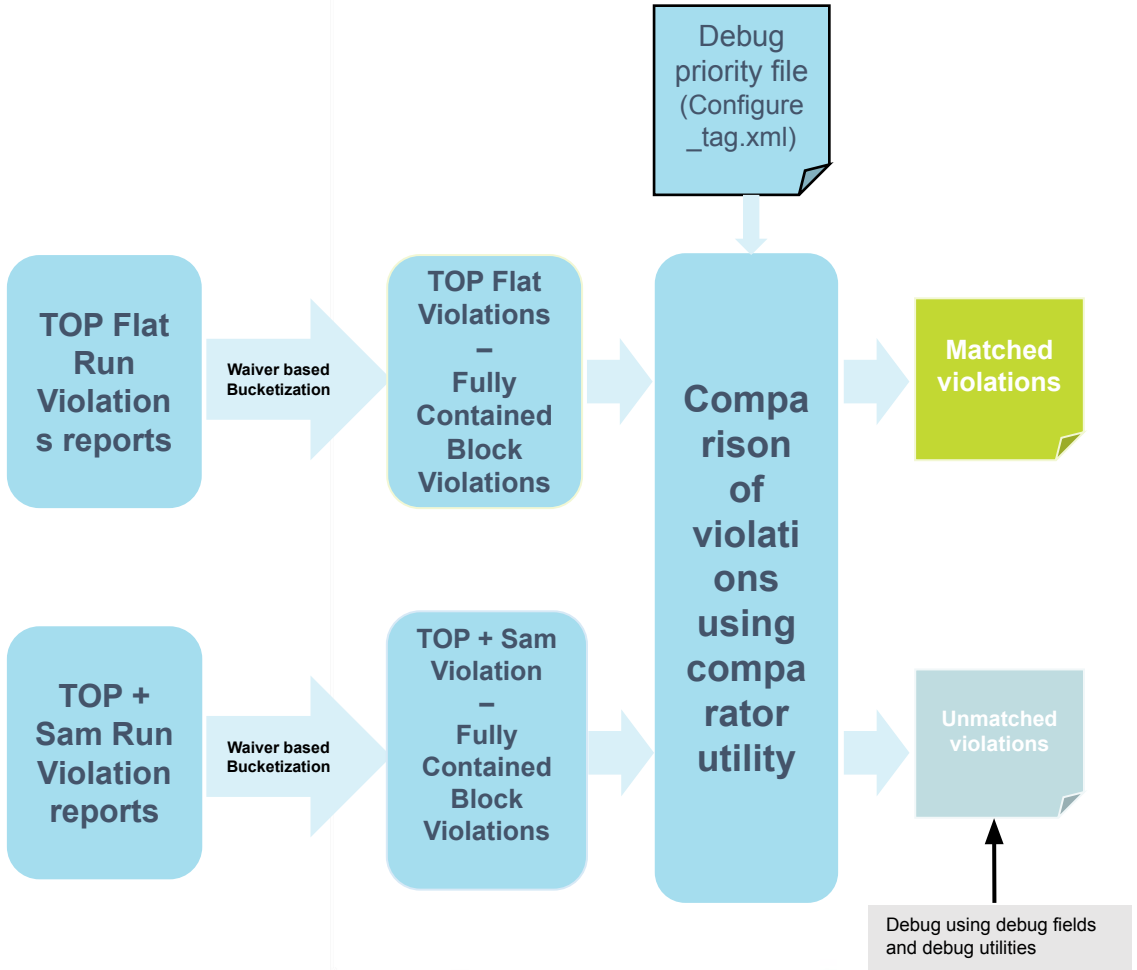
The steps encircled inside the dotted lines in the below flow diagram has been encompassed in the solution.



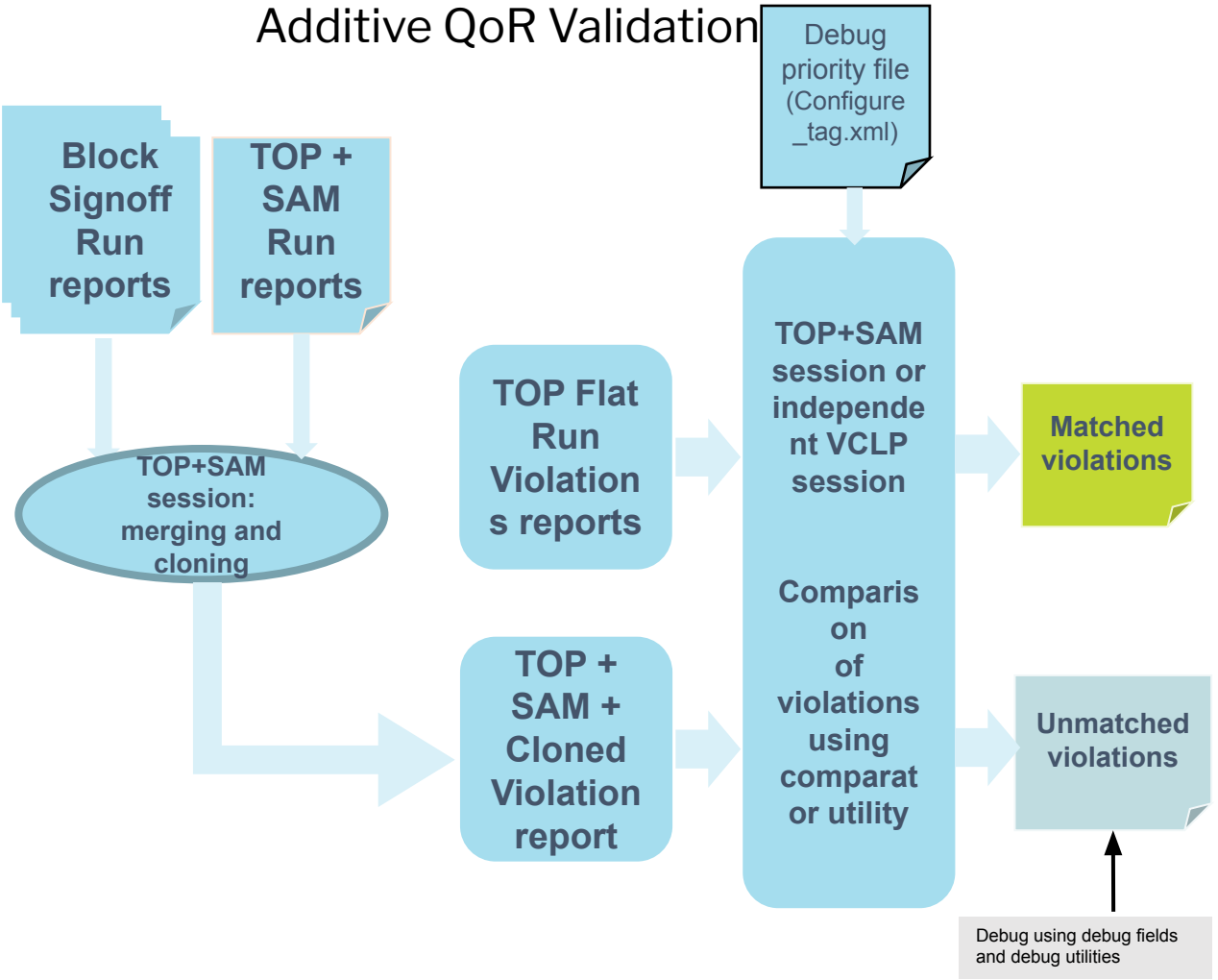


QoR Guarantee

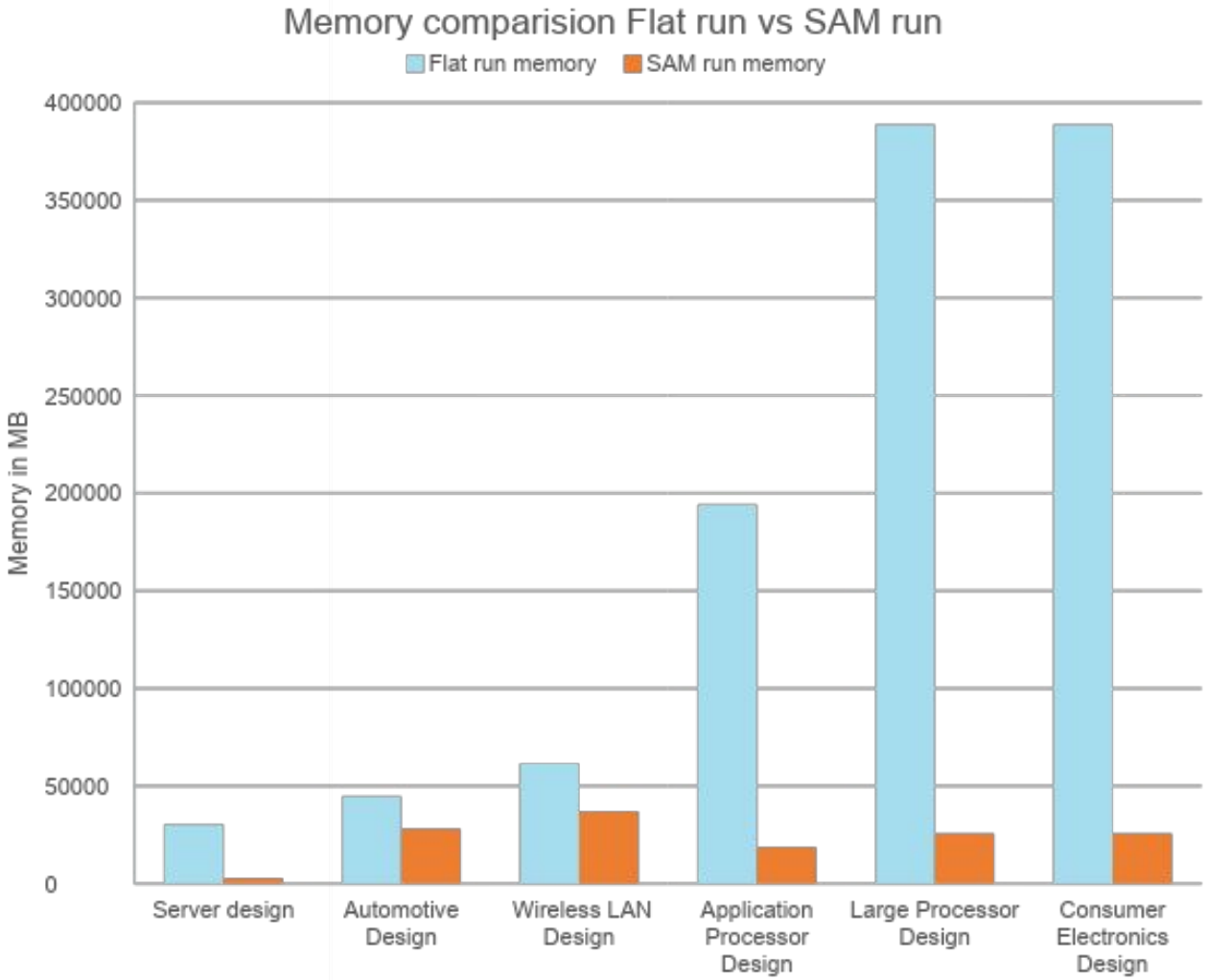
Subtractive QoR Validation

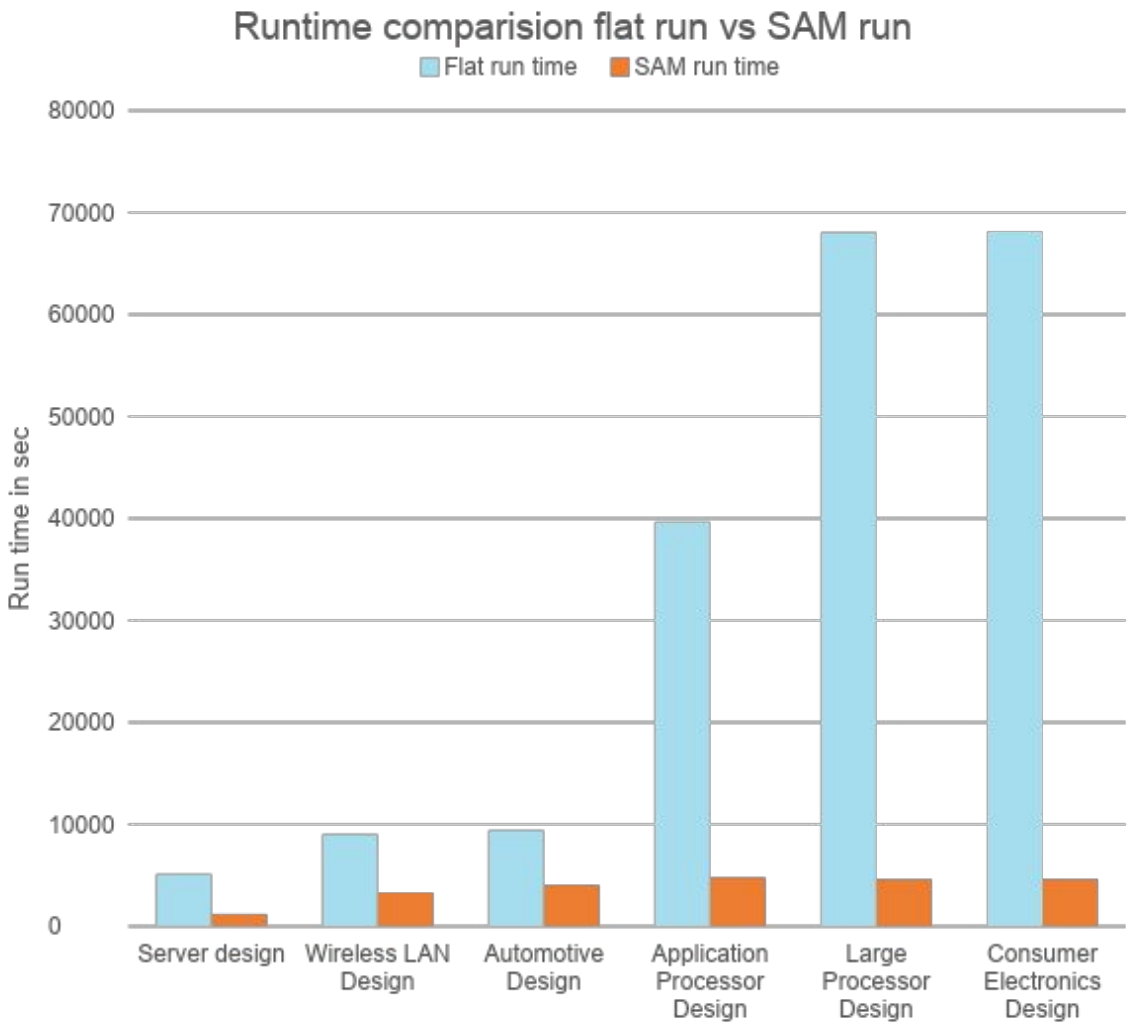


Additive QoR Validation



Results – Performance comparison





Summary

- Hierarchical signoff has become a necessity for today's memory and runtime intensive designs

- SAM flow maintains signoff accuracy and addresses capacity concerns
  - 1.5X to 15X gains when compared against full flat run
  - Larger the design size, better the gain
  - Additive and Subtractive flows guarantee signoff accuracy

- OTF SAM provides push button solution for easy adoption

- Further gains possible using custom flows on top of SAM flow
  - NPSR (Non Peripheral Supply Reduction) flow to solve complexity arising due to PST merging

- Testimony from Samsung:

"Maintaining performance and quality of results during low-power verification signoff is a must-have requirement," said Jung Yun Choi, vice president of Foundry Design Technology Team at Samsung Electronics. "Using the Signoff Abstract Model flow in the VC LP solution enables us to accelerate static low-power verification by 5X, and ensures high-quality QoR and signoff for our ASIC designs. With minimal changes to existing environment configuration, the hierarchical flow can be seamlessly adopted over several designs, effectively supporting the expedition of high-quality ASIC delivery."

https://news.synopsys.com/2019-11-07-Synopsys-VC-LP-for-Low-Power-Signoff-Verification-Delivers-Up-to-5X-Runtime-Gain-at-Samsung